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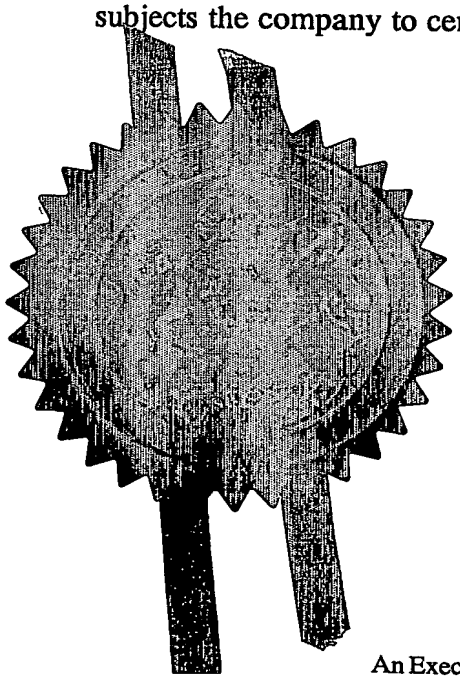

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Dated 28 October 2003

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2. Patent application number *(The Patent Office will fill in this part)* — 0223632.1 — 11 OCT 2002

3. Full name, address and postcode of the or of each applicant *(underline all surnames)* — AOTI OPERATING COMPANY, INC.
131 NW HAWTHORNE AVENUE
SUITE 207
BEND, OREGON 97701, US

Patents ADP number *(if you know it)* — 8138035002

If the applicant is a corporate body, give the country/state of its incorporation — DELAWARE, USA

4. Title of the invention — SEMICONDUCTOR TESTING INSTRUMENT

5. Name of your agent *(if you have one)* — NOVAGRAAF PATENTS LIMITED

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)* — THE CRESCENT
54 BLOSSOM STREET
YORK YO14 1AP

Patents ADP number *(if you know it)* — 08299166001

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7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application	Number of earlier application	Date of filing *(day / month / year)*

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   b) there is an inventor who is not named as an applicant, or
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Claim *(s)*	
Abstract	
Drawing *(s)*	5 + 5 RN

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Request for preliminary examination and search *(Patents Form 9/77)*	
Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(please specify)*	

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Signature NOVAGRAAF PATENTS LIMITED Date 10/10/2002

12. Name and daytime telephone number of person to contact in the United Kingdom PETER WILSON (DR) 01904 610586

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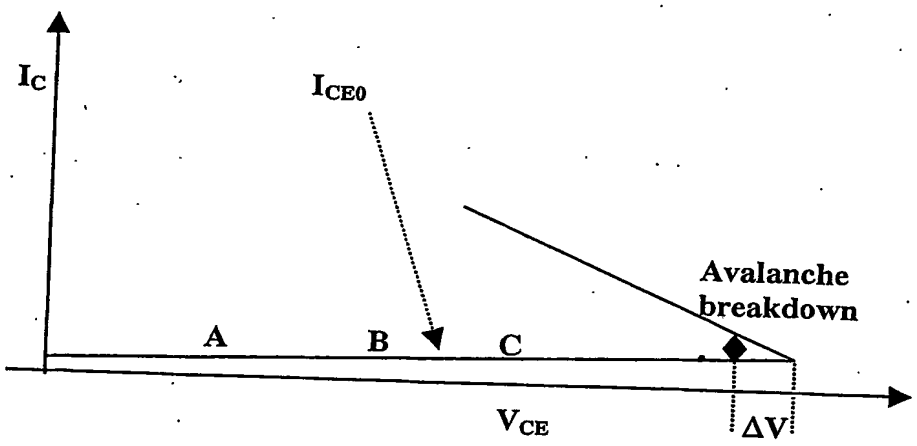

Figure 1

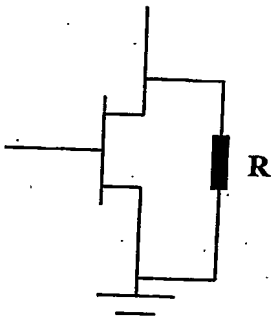

Figure 2

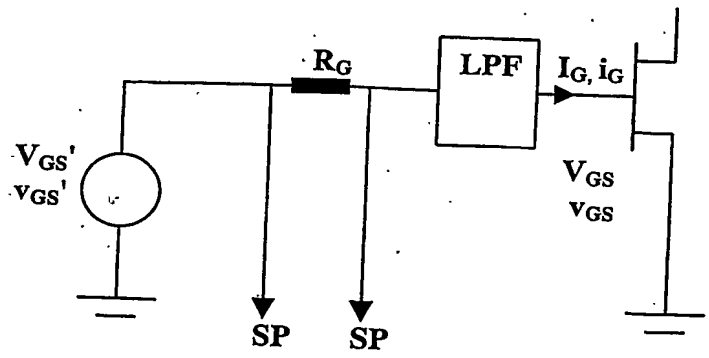

Figure 3

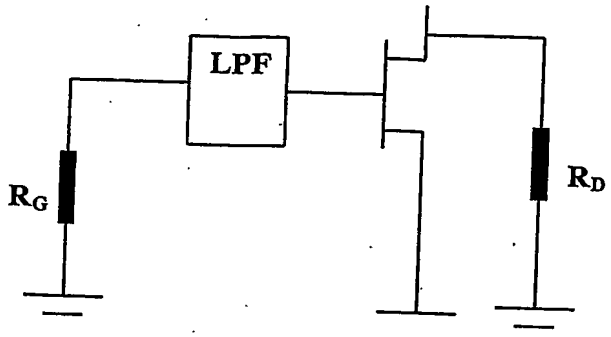

Figure 4

Input generator

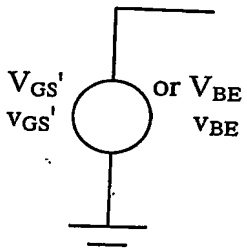

Figure 5

Input op amp

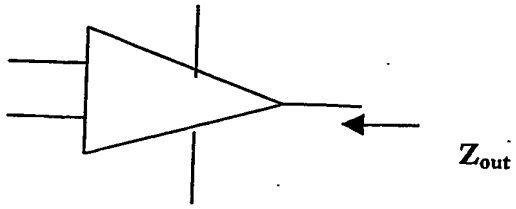

Figure 6

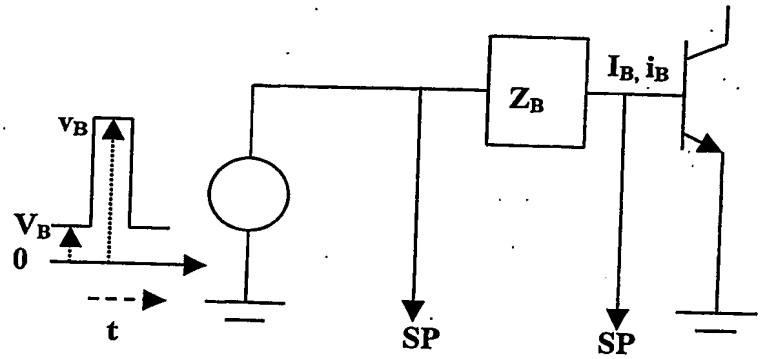

Figure 7

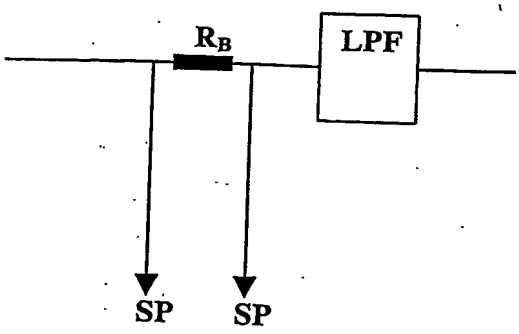

Figure 8

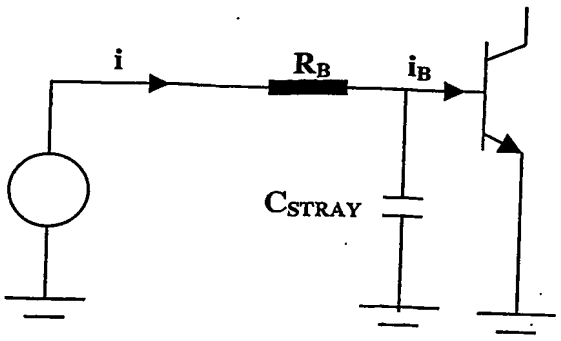

Figure 9

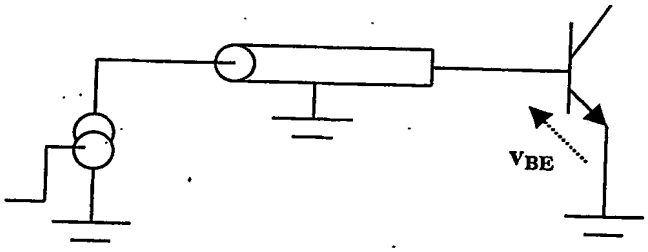

Figure 10

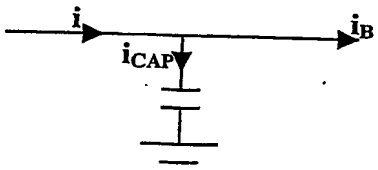

Figure 11

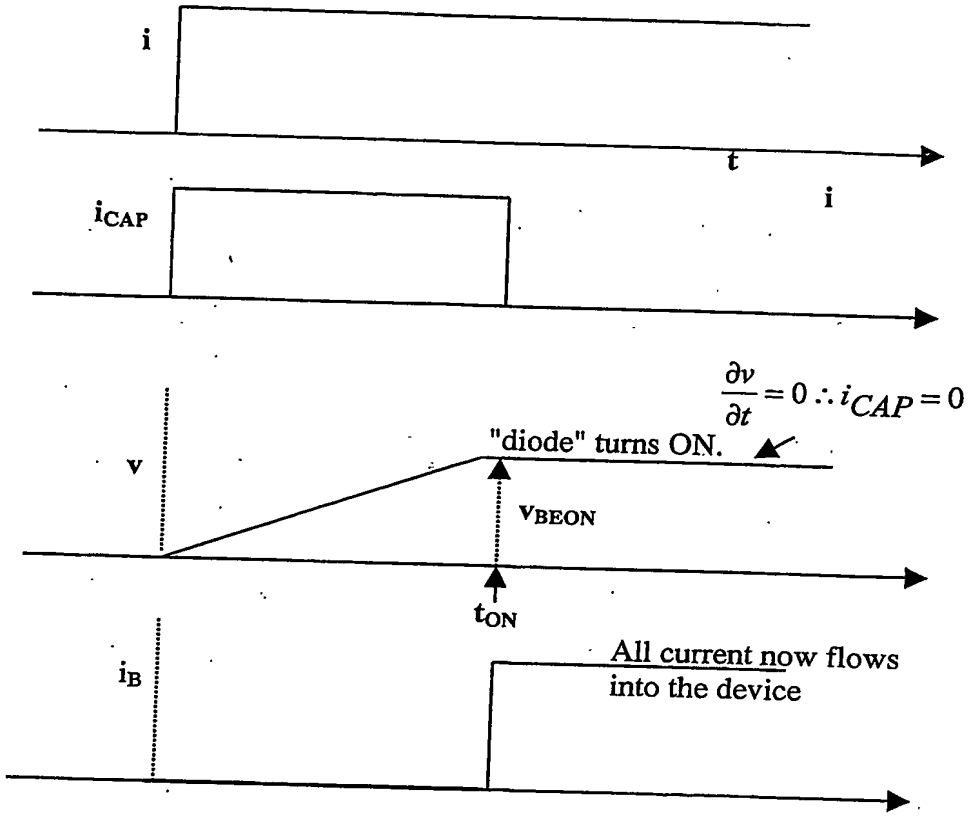
i
t
i
i_{CAP}
$\frac{\partial v}{\partial t} = 0 \therefore i_{CAP} = 0$
"diode" turns ON.
v
v_{BEON}
t_{ON}
i_B
All current now flows into the device

Figure 12

SEMICONDUCTOR TESTING INSTRUMENT

The present invention relates to a semiconductor testing instrument, and in particular to an instrument for determining the safe area of operation of such a device, especially of the bipolar type, and especially at RF frequencies and/or under large signal conditions. The invention also relates to a method of such measurement.

Increasingly, modern electronic systems rely upon semiconductor devices operated under large-signal conditions. For example, mobile phone handsets, power amplifiers, base stations, radars, missile guidance systems, electronic instruments, and other like electronic systems use semiconductor integrated circuits (ICs) or discrete devices which are designed to operate under such large signal conditions.

For semiconductor devices of all types, including transistor devices, semiconductor LEDs and lasers and other semiconductor devices, there is a thus a general requirement to be able to determine the dc safe area of operation (SOA), in the high-voltage low-current limit, without risking destruction of the device under test, and thus to identify the safe area of operation for the device.

This applies to most types of transistor devices (discrete or integrated) including, without limitation, those listed below, but is particularly the case for bipolar and like devices which are prone to undergo catastrophic avalanche breakdown outside the operational area.

- bipolar transistors: NPN and PNP devices.[1]
- silicon FETs including MOSFETs (metal-oxide-semiconductor field-effect transistors) and LDMOS (laterally diffused metal oxide semiconductor).[1]

- MESFETs (metal-electrode-semiconductor field-effect transistors. Most commonly GaAsFETs when fabricated in GaAs).[2]
- HEMTs (high electron mobility transistors).[2]
- HBTs (heterojunction bipolar transistors).[1,2]

Note that devices marked [1] are generally fabricated in silicon (Si), silicon-germanium (SiGe) or silicon carbide (SiC), whereas devices marked [2] are generally fabricated using high-electron mobility compound semiconductor materials such as gallium arsenide (GaAs) or indium phosphide (InP).

It is an object of the present invention to mitigate some or all of the above disadvantages.

It is a particular object of the present invention to provide a testing instrument and method for accurate determination of the dc safe area of operation (SOA), in the high-voltage low-current limit, without risking destruction of the device under test, and thus to identify the safe area of operation for the device under test.

In accordance with the invention at its broadest a device for determination of the dc safe area of operation of a semiconductor device under test comprises a means to apply an adjustable bias at the input of a device under test, whereby the means first applies a dc bias at a bias point within the safe operating limit, and then applies a variable bias comprising fast, superimposed rectangular bipolar pulses and the instrument further comprises means to measure the current response thereto so as to extrapolate a detailed I-V response in the vicinity of the safe operating limit.

In accordance with the principles of the invention a dc bias is applied by the instrument within the safe operating limit of the device under test in

conventional manner. A variable bias comprising fast, super imposed rectangular bipolar pulses is then applied by the instrument with the intention of taking the device under test beyond the operational limit. Conveniently, this is achieved in that the pulses are applied with progressively increasing amplitude.

This takes the device under test for a short period beyond the safe operating limit, and in its particular preferred application with bipolar and like devices, into the avalanche breakdown area. However, it is a characteristic feature of the instrument in accordance with the invention that the short pulse rates, combined with rapid measurement times, enable this breakdown area to be identified before catastrophic breakdown has time to occur in the device under test.

For accurate determination of the breakdown point, the above process may be repeated as an iterative succession. An initial dc bias is applied at a point known to be well within the safe operating area of the device under test. A pulsed bias is superimposed, and in particular a pulsed bias of progressively increased amplitude is superimposed. As incipient breakdown is detected the pulsed bias is removed. A second dc biasing point is determined in the vicinity of but safely below the breakdown point as identified by the first stage in the iterative process, and the process is repeated. After several iterations a very accurately determined breakdown point is obtained.

Thus, in accordance with the foregoing, the invention permits accurate and specific measurement of the safe operating area, and in particular of any catastrophic breakdown point, of a particular semiconductor device in non-destructive manner.

Preferably, the pulsed wave form is essentially critically damped so as to achieved a minimum rise time up to the point where the pulses become substantially flat. There is a further general requirement that the pulses to be applied must provide a high degree of isolation of the instrument from external influences that would otherwise degrade the performance.

The particular problem encountered at the high pulse frequencies required by the instrument of invention is that of applying a suitable biasing pulse, maintaining the pulse shape and integrity, and rapidly measuring current responses, whilst at the same time achieving device stability. At these frequencies, practical devices tend to undergo spurious oscillation when under test.

It has been suggested in the prior art that higher frequency pulses could be applied while keeping devices stable by use of a "bias tee". However, the capacitances within such as bias tee give the bias tee itself its own frequency response, which in practice limits the speed of the pulse which can be used. By contrast, in the present invention, fast stepped pulses in particular with pulse rates below about one μs and more preferably in some cases below 100 Ωs, are desired if avalanche effects are to be avoided.

In a particular embodiment of the invention, this is achieved in that the means to apply the adjustable bias at the input comprises a high stability voltage source serially connected to the input via a resistor, and preferably further serially connected through a low pass filter.

The power supply is selected to have a very low output impedance even at the high frequencies used to apply the test pulse.

The effect of this arrangement as incipient spurious oscillations arise will be understood. To spurious oscillation disturbances the near perfect power supply appears as a short. The circuit therefore functions in effect as a resistive termination, and it is well understood that such a resistive termination is effective as a means of unconditionally stabilising a transistor or like device.

The resistor used to achieve this resistive termination must be very low in parasitic reactances. Device stabilisation is preferably achieved by a resistance in the range of some 10s of Ω to 100s of Ω, for example 50 Ω to 500 Ω.

The inclusion of an optional low pass filter represents a second stabilisation measure which increases the effectiveness of stabilisation at input. The low pass filter is selected such as to be effectively transparent at the pulse rates and rise times under test, but act to inhibit time dependent variations in current or voltage at higher oscillation frequencies.

Conveniently, the low pass filter comprises a shunt capacitor across the resistance followed by a series inductor.

In accordance with a further aspect of the invention, a method for determination of the dc safe area of operation of a semiconductor device under test comprises comprises applying a dc bias at the input of the device under test to determine a bias point near to the safe operating limit, applying an adjustable bias at the input of the device under test comprising fast, super imposed rectangular bipolar pulses, rapidly measuring the current response thereto at both the input and output, extrapolating from the responses a detailed I-V response for the device in the vicinity of the safe operating limit.

Preferred features of the method and preferred or necessary parameters for the bipolar pulse, pulse rates, measurement times etc will be understood by analogy with the foregoing.

The invention will now be described by way of example only with reference to Figures 1 to 13 of the accompanying drawings wherein:

Figure 1 is an illustration of the I-V characteristics for a typical bipolar device;
Figure 2 illustrates the principle of resistively terminating a FET;
Figure 3 illustrates an arrangement for an embodiment of the invention supplying power at a gate of an FET;
Figure 4 illustrates an effective equivalent circuit to Figure 3 as far as spurious noise oscillations are concerned;
Figures 5 and 6 illustrate preferred pulse generators;
Figures 7 and 8 illustrates an example circuit especially suited for application of the invention to a bipolar transistor;
Figure 9 illustrates the problem of stray shunt capacitance;
Figures 10-12 illustrate an embodiment of the invention adapted to produce particularly short pulse lengths of the order of 1 ns.

I-V characteristics for a typical bipolar semiconductor device under test are shown in figure 1. I_{CE0} is the current flowing from collector-to-emitter with the base open circuit ($i_B = 0$). The I-V curve illustrates the catastrophic avalanche breakdown which is a particular characteristic of bipolar devices. Some FETs and HEMTs collapse in a similar manner. The invention is particularly applicable to the detection of the safe operating limit in devices which undertgo this or another form of runaway breakdown at the edge of that limit, and is discussed by way of example in relation to a bipolar device, but is not limited to such use.

The requirement is to detect the onset of avalanche breakdown very rapidly, and then reduce the voltage so it does not occur. For this the following approach is adopted.

The device-under-test is biased under DC conditions at the point marked ♦ on the curve in figure 1. This is within a fraction of a volt of breakdown and the voltage difference is ΔV. This remaining voltage ΔV is then applied under pulse conditions.

The key is to keep the pulse and sampling times short enough to detect and catch the avalanche before it becomes destructive, i.e. before runaway sets in.

In this approach it is important to start conservatively. Referring to Figure 1, the process is carried out iteratively from a series of base bias points succesively nearer to the breakdown point.

The process begins at test point A and then a steady increase in the pulse amplitude is applied until breakdown just starts to occur. At this point the pulse must be rapidly removed, but the breakdown voltage will now be approximately known so it is possible to increase the voltage such that test point B (TPB) is reached. Now there is a new, reduced, ΔV between this TPB voltage and breakdown and the process is repeated - setting to test point C, etc. - until the DC test point voltages converge at breakdown. Then the breakdown voltage is accurately known.

In the example this procedure is followed manually but rapidly. An automated device adapted to perform the iteration without user intervention could be envisaged.

A test device in accordance with the invention applies the DC bias and applies pulses at this bias point to the device-under-test. However, parasitic impedances arise in series with the source or (base). Also there are parasitic impedances from these terminals to ground. These impedances arise inevitably from the device itself, from jigs supporting the device-under-test, from the measuring instrument, connecting cable, etc.). The existence of these parasitic impedances means that the device-under-test is subject to a risk of oscillation.

Meaningful measurements cannot proceed with an oscillating device. The question therefore arises as to how to achieve device stability. With the device in accordance with the invention arrangements are made to precisely ensure stability. How this is achieved is discussed below.

In order to unconditionally stabilise a transistor microwave engineers tend naturally to resistively terminate the output of the device - drain to ground for an FET and collector to ground for a bipolar. This principle is illustrated in figure 2. Although an FET transistor is shown it will be understood that the same approach is also applicable by analogy to a bipolar type device.

It is a key feature of the preferred embodiment of the present invention that the testing device is adapted to mimic this principle.

Figure 3 illustrates how this is achieved in the example device on the input side (gate or base). The choice of R_G is critical, being some tens to hundreds of ohms and *very* low in parasitic reactances. A very important feature is that the introduction of the low-pass filter (LPF) represents a second stabilisation measure.

As far as spurious "incipient" oscillation or noise signals are concerned the circuit appears as shown in Figure 4 (in which the output is also shown as resistively terminated by the resistor R_D).

The low-pass filter (LPF) has to be transparent at the pulse rates and rise times attendant to the measurement, but also must be such as to quench and inhibit time-dependent variations in current or voltage at higher (oscillation) frequencies.

In practice the LPF is realised simply as a shunt capacitor across R_G followed by a series inductor in the gate (or base) lead.

This arrangement:

- Keeps the device under test stable.
- Allows input and output conduction currents to be measured under dc and dynamic conditions.
- Allows dc biases and pulses to be applied simultaneously to the device under test.
- Allows fast (few tens of nanoseconds rise time) pulses to be applied.
- Provides a measure of buffering or isolation of the device under test, which preserves the pulse shape and integrity.
- Provides a measure of protection from device destruction by current runaway - especially with bipolar devices.
- Provides a measure of short-circuit protection for the instrument.

There are also important special aspects regarding the pulse generator. This is indicated in Figure 5. This generator is realised in practice in the form of an operational amplifier (op amp), as shown in Figure 6.

The important requirement is that for the op amp the output impedance Z_{out} must be kept extremely low - even at RF and microwave frequencies. For this the op amp need to be specially selected.

The consequence is that this scheme allows short pulses to be generated - down to a few tens of nanoseconds (ns).

The foregoing examples have been given in terms of FET transistors allowing good illustration of the principles of resistive termination. However, the invention is particularly applicable to bipolar transistors and the like which undergo catastrophic avalanche failure. Bipolar Transistor Measurements present particular difficulties. Figures 7 and 8 illustrate the principles of an embodiment of the invention in measuring, at constant base current I_B, the dynamic I-V characteristics of bipolar transistors - which are notoriously unstable.

There are two important issues;

(i) How to measure the dynamic I-V conduction characteristics with I_B constant as parameter, whilst keeping the device stable.

(ii) Defining the measurement conditions for valid measurement of the dynamic I-V conduction characteristics uncorrupted by the reactive effects.

Considering issue (ii) first of all. The measurement conditions are satisfied by maintaining the pulse length greater than a time as defined by the following inequality:

$$t_{pulse} \geq t_{ON} = \frac{(\beta+1) i_{BSTEP}}{2\pi f_T \left(\frac{kT}{q}\right)} R_B \ell n \left[1 + \frac{v_{BEON}}{i_{BSTEP} R_B}\right]$$

In which: t_{ON} is the time required to fully turn the transistor on, β is the DC collector-to-base current ratio, f_T is the current transition frequency and all the remaining quantities are readily known. At normal ambient temperature ("room" temperature) T = 298K and the kT/q ratio is 0.025V.

There is one connection approach that might ideally be desired - but which cannot be achieved – which is to drive the base input from a constant current source. Microwave and RF engineers, will understand that this cannot practicably be achieved. At the high frequencies associated with the very short pulses only S-parameters may be used and these demand matched terminations - not the open or short-circuit approximations used with h-parameters or y-parameters, etc.

(Under small-signal linearized conditions one can measure S-parameters and then transform the results into h, y, z ABCD or other sets of parameters. However, under large-signal conditions this cannot be done.)

So, for measuring a bipolar transistor, what has to be established is the type of circuit indicated in Figure 7. As before, sampling points SP are immediately followed by A > D converters within the measuring instrument.

Regarding Z_B, this required series impedance is:

(a) realistic in the practical case, and
(b) needed for device under test stability.

With Z_B it is now possible to measure directly what is required, as follows:

Z_B is realised as resistor R_B in series with a low-pass filter (LPF), indicated in Figure 8.

R_B is typically a few hundreds of ohms in value and it must also be very low in parasitic reactance's. Note that the value range is around an order-of-magnitude larger than for R_D described in conjunction with measurements on FETs, see above. The LPF has to be "transparent" at the pulse rates and rise times in use, In this method fast-sampling is used at the SP points (i.e. A-D5 and A-D6) and iterate V_B, v_B (digitally) until I_B, i_B are as set - or as desired.

Figure 9 illustrates an embodiment of the device specifically adapted for measurement at very low i_B values - in the region of 1μA order of magnitude.

The stray instrument capacitance C_{STRAY} represents a problem and special low-capacitance buffering techniques, internal to the measuring instrument, are required to keep the effective stray capacitance low - down to the order of a few pF. As this stray capacitance is made smaller, so i_B can be set ever smaller - within known accuracy limits.

Figure 10 illustrates an embodiment of the device specifically adapted for pulse lengths having an order of magnitude of 1 nanosecond (1 ns).

A problem arises at such short pulse lengths if a connection is made using a cable run that is predominantly capacitive, as shown in Figure 10. This is approximately equivalent to the simple circuit shown in Figure 11 which shows the current i_{CAP} that flows in the capacitive element of the cable.

The key aspects are:

(I) Start from $v_{BE} = 0$ (i.e. $i_B = 0$), then:

(II) Turn the pulse on - from a current generator source.

The waveforms of Figure 12 show the effects - remembering that $i = C\frac{dv}{dt}$

The time t_{ON} can be ascertained by continually sampling (since when $i_B = 0$, $i_C = 0$). The sample acquisition time is around 1 to 2 ns. Therefore it is possible to sample i_C and this enables measurements at pulse lengths of the order of 1 ns.

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